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1 A VLSI motion estimator for video image compression
Chen-Mie Wu; Ding-Kuen Yeh;
Consumer Electronics, IEEE Transactions on , Volume: 39 Issue: 4 , Nov 1993
Page(s): 837 -846

[Abstract] [PDF Full-Text (588 KB)] **IEEE JNL**

2 A real time MPEG2 main profile, main level motion-estimator chipset
Pacalet, R.; Lafage, A.; Darbel, N.; Tychon, P.; Bellier, A.; Dejean, C.; Dutein, C. E.; Haas, S.; Laberl, S.; Lievre, B.; Simon, L.; Talayssat, J.;
Solid-State Circuits Conference, 1997. Digest of Technical Papers. 44th ISSCC., 1 IEEE International , 6-8 Feb. 1997
Page(s): 260 -261, 469

[Abstract] [PDF Full-Text (908 KB)] **IEEE CNF**

3 A quality measure for compressed image sequences based on an eye-movement compensated spatio-temporal model
Westen, S.J.P.; Lagendijk, E.L.; Biemond, J.;
Image Processing, 1997. Proceedings., International Conference on , Volume: 1 , 26-29 Oct. 1997
Page(s): 279 -282 vol.1

[Abstract] [PDF Full-Text (516 KB)] **IEEE CNF**

4 Performance of motion estimators over MPEG coder considering frame analysis
de Oliveira, G.C.; Alcaim, A.;

Global Telecommunications Conference, 1998. GLOBECOM 98. The Bridge to Global Integration. IEEE , Volume: 1 , 8-12 Nov. 1998
Page(s): 50 -53 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(236 KB\)\]](#) **IEEE CNF**

5 One-dimensional full search motion estimation algorithm for video coders
Chen, M.-J.; Chen, L.-G.; Chiueh, T.-D.;
Circuits and Systems for Video Technology, IEEE Transactions on , Volume: 4 Issue: 4 , Oct. 1994
Page(s): 504 -509

[\[Abstract\]](#) [\[PDF Full-Text \(440 KB\)\]](#) **IEEE JNL**

6 Flexible VLSI architecture of motion estimator for video image compression
Seung Hyun Nam; Moon Key Lee;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on , Volume: 43 Issue: 6 , June 1996
Page(s): 467 -470

[\[Abstract\]](#) [\[PDF Full-Text \(384 KB\)\]](#) **IEEE JNL**

7 A cascading MRVQ-DCT scheme for the compression of sequence images
Shih-Yu Huang; Jia-Shung Wang;
Image Processing, IEEE Transactions on , Volume: 6 Issue: 8 , Aug. 1997
Page(s): 1188 -1192

[\[Abstract\]](#) [\[PDF Full-Text \(408 KB\)\]](#) **IEEE JNL**

8 Motion estimation using a complex-valued wavelet transform
Magarey, J.; Kingsbury, N.;
Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on] , Volume: 46 Issue: 4 , April 1998
Page(s): 1069 -1084

[\[Abstract\]](#) [\[PDF Full-Text \(808 KB\)\]](#) **IEEE JNL**

9 An optimal quadtree-based motion estimation and motion-compensated interpolation scheme for video compression
Schuster, G.M.; Katsaggelos, A.K.;
Image Processing, IEEE Transactions on , Volume: 7 Issue: 11 , Nov. 1998
Page(s): 1505 -1523

[Abstract] [PDF Full-Text (556 KB)] **IEEE JNL**

10 A simple recursive motion estimation technique for compression of HC signals

de With, P.H.N.;

Image Processing and its Applications, 1992., International Conference on , 7-9 / 1992

Page(s): 417 -420

[Abstract] [PDF Full-Text (260 KB)] **IEE CNF**

11 Multi-level pixel difference classification methods

Chan, Y.; Kung, S.Y.;

Image Processing, 1995. Proceedings., International Conference on , Volume: 3 , 23-26 Oct. 1995

Page(s): 252 -255 vol.3

[Abstract] [PDF Full-Text (580 KB)] **IEEE CNF**

12 A programmable motion estimation processor for full search block matching

Pirson, A.; Yassa, F.; Paul, P.; Canfield, B.; Rominger, F.; Graf, A.; Teichner, D.; Acoustics, Speech, and Signal Processing, 1995. ICASSP-95., 1995 International Conference on , Volume: 5 , 9-12 May 1995

Page(s): 3283 -3286 vol.5

[Abstract] [PDF Full-Text (340 KB)] **IEEE CNF**

13 Spatial frequency based motion estimation for image sequence compression

Menezes, V.; Nandy, S.K.; Mitra, B.;

High Performance Computing, 1996. Proceedings. 3rd International Conference o 19-22 Dec. 1996

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[Abstract] [PDF Full-Text (456 KB)] **IEEE CNF**

14 Low-complexity global motion estimation from P-frame motion vector: MPEG-7 applications

Smolic, A.; Hoeynck, M.; Ohm, J.-R.;

Image Processing, 2000. Proceedings. 2000 International Conference on , Volume 10-13 Sept. 2000

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[\[Abstract\]](#) [\[PDF Full-Text \(464 KB\)\]](#) **IEEE CNF**

15 Mesh based video coding at very low bitrate

Laurent, N.; Robert, G.;

Image Processing, 2000. Proceedings. 2000 International Conference on , Volume 6
10-13 Sept. 2000

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[\[Abstract\]](#) [\[PDF Full-Text \(364 KB\)\]](#) **IEEE CNF**

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| 1 | Long instruction word controlling plural independent processor operations | 708/603 | | |
| 2 | Method and apparatus for eliminating the transpose buffer during a decomposed forward or inverse 2-dimensional discrete cosine transform through operand decomposition, storage and retrieval | 708/402 | 708/401 | |
| 3 | Method for choosing rate control parameters in motion-compensated transform-based picture coding scheme using non-parametric technique | 382/239 | 348/416.1; 382/238; 382/250; 382/251 | |
| 4 | Video data encoder and decoder | 375/240.03 | 375/240.16; 382/232; 382/240; 382/246 | |
| 5 | Long instruction word controlling plural independent processor operations | 708/524 | 708/620 | |
| 6 | Method, apparatus and system for sum of plural absolute differences | 708/709 | 708/440; 708/670; 708/710; 712/200 | |
| 7 | Instruction having bit field designating status bits protected from modification corresponding to arithmetic logic unit result | 712/226 | 708/525; 712/221; 712/224 | |
| 8 | Division by iteration employing subtraction and conditional source selection of a prior difference or a left shifted remainder | 708/650 | 708/620 | |
| 9 | Three input arithmetic logic unit with barrel rotator | 708/236 | 708/209; 712/221 | |
| 10 | Method and apparatus for performing two pass quality video compression through pipelining and buffer management | 382/236 | | |
| 11 | Three input arithmetic logic unit with shifter | 712/20 | | |

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| | Title | Current OR | Current XRef | Retrieval Classif |
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| 12 | Rotation register for orthogonal data transformation | 712/32 | 708/500 | |
| 13 | Memory store from a register pair conditional upon a selected status bit | 712/225 | 712/226; 712/234 | |
| 14 | Long instruction word controlling plural independent processor operations | 708/620 | 708/518; 708/628 | |
| 15 | Data processing apparatus, system and method for if, then, else operation using write priority | 712/226 | 712/225; 712/234 | |
| 16 | Method and apparatus for eliminating the transpose buffer during a decomposed forward or inverse 2-dimensional discrete cosine transform through operand decomposition storage and retrieval | 709/247 | 710/1; 710/29; 710/52; 710/58; 712/220 | |
| 17 | Method, apparatus and system forming the sum of data in plural equal sections of a single data word | 712/32 | 708/490; 708/500; 708/670 | |
| 18 | Three input arithmetic logic unit with shifter and/or mask generator | 712/221 | 708/209; 712/223 | |
| 19 | Three input arithmetic logic unit capable of performing all possible three operand boolean operations with shifter and/or mask generator | 712/221 | 708/230; 708/236 | |
| 20 | Method and apparatus for interleaving and de-interleaving YUV pixel data | 345/603 | 345/530; 345/555; 707/101; 711/157 | |
| 21 | Three input arithmetic logic unit with shifter and mask generator | 712/221 | 708/236; 712/224 | |
| 22 | System and method for performing motion estimation with reduced memory loading latency | 375/240.15 | 348/699; 375/240.24 | |
| 23 | Three input arithmetic logic unit with barrel rotator and mask generator | 712/221 | 708/230; 712/224 | |

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| 24 | Apparatus and system for sum of plural absolute differences | 712/221 | 708/236; 712/224 | |
| 25 | Video encoder/decoder system | 375/240.22 | 382/253 | |
| 26 | Arithmetic logic unit with conditional register source selection | 712/209 | 708/490 | |
| 27 | Base address generation in a multi-processing system having plural memories with a unified address space corresponding to each processor | 711/147 | 711/148; 711/152; 711/153 | |
| 28 | Transparent block skipping in object-based video coding systems | 382/243 | 382/239 | |
| 29 | Long instruction word controlling plural independent processor operations | 708/620 | 708/628 | |
| 30 | Hardware branching employing loop control registers loaded according to status of sections of an arithmetic logic unit divided into a plurality of sections | 712/221 | 712/223; 712/241 | |
| 31 | Method, apparatus and system forming the sum of data in plural equal sections of a single data word | 712/224 | 708/490; 708/518; 712/221; 712/36 | |
| 32 | Address generator employing selective merge of two independent addresses | 711/211 | 345/504; 345/572; 711/220 | |
| 33 | Memory store from a selected one of a register pair conditional upon the state of a selected status bit | 712/245 | 712/225 | |
| 34 | Three input arithmetic logic unit with shifting means at one input forming a sum/difference of two inputs logically anded with a third input logically ored with the sum/difference logically anded with an inverse of the third input | 712/221 | 708/209; 708/490; 712/223 | |
| 35 | Method apparatus and system for correlation | 708/525 | 712/221 | |

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| 36 | Conditional processor operation based upon result of two consecutive prior processor operations | 712/234 | 712/20 | |
| 37 | Method for rounding using redundant coded multiply result | 708/493 | | |
| 38 | Iterative division apparatus, system and method employing left most one's detection and left most one's detection with exclusive or | 708/655 | | |
| 39 | Method, apparatus and system for multiply rounding using redundant coded multiply result | 708/551 | 708/493 | |
| 40 | Arithmetic logic unit having plural independent sections and register storing resultant indicator bit from every section | 712/221 | 708/209; 708/230; 708/525; 708/670 | |
| 41 | Three input arithmetic logic unit with controllable shifter and mask generator | 708/230 | 712/200 | |
| 42 | Packed word pair multiply operation forming output including most significant bits of product and other bits of one input | 712/208 | 708/625 | |
| 43 | Three input arithmetic logic unit with mask generator | 712/36 | 345/501; 712/34 | |
| 44 | Three input arithmetic logic unit forming mixed arithmetic and boolean combinations | 708/670 | 708/236 | |
| 45 | Iterative division apparatus, system and method employing left most one's detection and left most one's detection with exclusive OR | 708/655 | | |
| 46 | Three input arithmetic logic unit with mask generator | 712/36 | 345/501; 712/34 | |
| 47 | Huffman encoding method, circuit and system employing most significant bit change for size detection | 341/65 | | |

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| 52 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 5465224 A | 19951107 | |
| 53 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 5446651 A | 19950829 | |
| 54 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 5442581 A | 19950815 | |
| 55 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 5420809 A | 19950530 | |
| 56 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | US 5091782 A | 19920225 | |

| | Title | Current OR | Current XRef | Retrieval Classif |
|----|--|------------|------------------------------------|-------------------|
| 48 | Long instruction word controlling plural independent processor operations | 712/203 | 708/524; 712/24 | |
| 49 | Three input arithmetic logic unit employing carry propagate logic | 708/709 | | |
| 50 | Three input arithmetic logic unit forming the sum of a first input anded with a first boolean combination of a second input and a third input plus a second boolean combination of the second and third inputs | 708/230 | | |
| 51 | Huffman decoding method, circuit and system employing conditional subtraction for conversion of negative numbers | 341/65 | | |
| 52 | Three input arithmetic logic unit forming the sum of a first Boolean combination of first, second and third inputs plus a second Boolean combination of first, second and third inputs | 708/236 | 708/670 | |
| 53 | Split multiply operation | 708/630 | | |
| 54 | Iterative division apparatus, system and method forming plural quotient bits per iteration | 708/653 | 708/650 | |
| 55 | Method of operating a data processing apparatus to compute correlation | 708/200 | 708/445 | |
| 56 | Apparatus and method for adaptively compressing successive blocks of digital video | 348/400.1 | 375/240.16; 382/236; 382/239 | |

| | Inventor | S | C | P | 2 | 3 | 4 | 5 | Image Doc. Displayed | PT |
|----|-----------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|-------------------------|--------------------------|
| 48 | Guttag, Karl M. et al. | <input type="checkbox"/> | | <input type="checkbox"/> |
| 49 | Guttag, Karl M. et al. | <input type="checkbox"/> | | <input type="checkbox"/> |
| 50 | Guttag, Karl M. et al. | <input type="checkbox"/> | | <input type="checkbox"/> |
| 51 | Read, Christopher J. et al. | <input type="checkbox"/> | | <input type="checkbox"/> |
| 52 | Guttag, Karl M. et al. | <input type="checkbox"/> | | <input type="checkbox"/> |
| 53 | Moyse, Phillip et al. | <input type="checkbox"/> | | <input type="checkbox"/> |
| 54 | Poland, Sydney W. | <input type="checkbox"/> | | <input type="checkbox"/> |
| 55 | Read, Christopher J. et al. | <input type="checkbox"/> | | <input type="checkbox"/> |
| 56 | Krause, Edward A. et al. | <input type="checkbox"/> | | <input type="checkbox"/> |